AMENDMENTS TO THE CLAIMS

Claims 1-38 (cancelled)

Claim 39. (previously presented): A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level;

wherein said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level.

Claim 40 (cancelled).

Claim 41. (previously presented): The capacitor according to claim 39, wherein said ion implantation doped BST thin film material is doped with a dopant selected from the group consisting of barium, strontium and titanium.

Claim 42. (previously presented): The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

Claim 43. (previously presented): The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is doped with Ti.

Claim 44. (previously presented): The capacitor according to claim 43, wherein said ion implantation doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

Claim 45. (previously presented): The capacitor according to claim 44, wherein the ratio of Ba to Sr is about 70:30.

Claim 46 (previously presented): The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is included in a DRAM cell.

Claim 47 (cancelled).

Claim 48. (previously presented): A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level;

wherein said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level; and

a capping layer provided over at least a portion of said ion implantation doped BST thin film material.

Claim 49 (cancelled).

Claim 50. (previously presented): The capacitor according to claim 48, wherein said ion implantation doped BST thin film material is doped with a dopant selected from the group consisting of barium, strontium and titanium.

Claim 51. (previously presented): The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

Claim 52. (previously presented): The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is doped with Ti.

Claim 53. (previously presented): The capacitor according to claim 52, wherein said ion implantation doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

Claim 54. (previously presented): The capacitor according to claim 53, wherein the ratio of Ba to Sr is about 70:30.

Claims 55 (previously presented): The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is included in a DRAM cell.

Claims 56-73 (cancelled).

Claim 74. (sixth amended): An integrated circuit capacitor device comprising:

a first electrode having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level;

wherein said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level; and

a second electrode provided on said ion implantation doped BST high dielectric thin film material.

Claim 75. (original): The integrated circuit capacitor device according to claim 74, wherein said dopants are selected from the group consisting of barium, strontium and titanium.

Claim 76. (original): The integrated circuit capacitor device according to claim 75, wherein said doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba, and Sr.

Claim 77. (original): The integrated circuit capacitor device according to claim 75, wherein said doped BST high dielectric thin film material is doped with Ti.

Claim 78. (original): The integrated circuit capacitor device according to claim 76, wherein said doped BST high dielectric thin film material is doped with Ti to maintain a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

Claim 79. (original): The integrated circuit capacitor device according to claim 78, wherein the ratio of Ba to Sr is about 70:30

Claim 80. (original): The integrated circuit capacitor device according to claim 74, wherein said first and second electrodes are selected from the group consisting of Pt, Ru, Ir, Pd, Au ruthenium oxides, and iridium oxides.

Claim 81. (original): The integrated circuit capacitor device according to claim 74, wherein said integrated circuit capacitor is a container capacitor.

Claim 82. (previously presented): The integrated circuit capacitor device according to claim 74, wherein said integrated circuit capacitor is formed over a stud.

Claim 83. (previously presented): The integrated circuit capacitor device according to claim 74, wherein said integrated circuit capacitor is fabricated in a DRAM cell.

Claim 84-93 (cancelled).

Claim 94. (previously presented): A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation doped high dielectric constant thin film material, said high dielectric thin film material having a general formula of ABO_3 and having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level,

wherein said ion implantation doped high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level.

Claim 95. (previously presented): The capacitor according to claim 94, wherein A of said formula ABO_3 is selected from the group comprising Ba, Bi, Sr, Pb, Ca, La, and any combination thereof.

Claim 96. (amended): The capacitor according to claim 94, wherein B of said formula ABO_3 is selected from the group comprising ~~Pt~~ Ti, Zr, Ta, Mo, W, Nb, and any combination thereof.

Claim 97. (amended): The capacitor according to claim 96 ~~94~~, wherein said ion implantation doped high dielectric constant thin film material contains a percentage of ~~B~~ Ti of approximately 50% to approximately 53.5% throughout said high dielectric constant thin film material.